



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant: Leonard Forbes et al.

Title: TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE

Docket No.: 303.324US4

Serial No.: 09/691,004

Filed: October 18, 2000

Due Date: August 20, 2002

Examiner: Johannes P. Mondt

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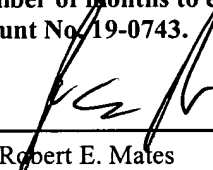
Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ A return postcard.
- ☒ An Amendment and Response (13 Pages).
- ☒ A Supplemental Information Disclosure Statement (1 pg.), Form 1449 (1 pg.), and copies of 7 cited references.
- ☒ A check in the amount of \$180.00 to cover the fee for consideration of Information Disclosure Statement under 97(c).
- ☒ A Copy of the Forms 1449 filed on October 18, 2000 (9 pgs) and copies of the non-patent literature listed on the 1449 form filed October 18, 2000.

Please consider this a **PETITION FOR EXTENSION OF TIME** for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
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By: 
Atty: Robert E. Mates
Reg. No. 35,271

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 20th day of August, 2002.

Amy Moriarty
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